FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20838-1E

FLASH MEMORY

CMOS

2 M (256 K × 8/128 K × 16) BIT

MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

■ FEATURES

- **Single 5.0 V read, program, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
  44-pin SOP (Package suffix: PF)
  48-pin TSOP (I) (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
- **Minimum 100,000 write/erase cycles**
- **High performance**
  90 ns maximum access time
- **Sector erase architecture**
  One 16K byte, two 8K bytes, one 32K byte, and three 64K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  TA = Top sector
  BA = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically write and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program of erase cycle completion.
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Hardware $\overline{\text{RESET}}$ pin**
  Resets internal state machine to the read mode.
- **Sector protection**
  Hardware method disables any combination of sectors from write or erase operations
- **Temporary sector groups unprotection**
  Hardware method temporarily enable any combination of sectors from write or erase operations

(Continued)

MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

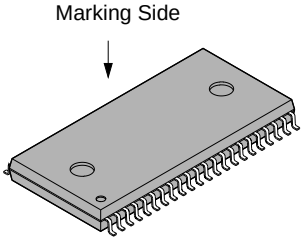
(Continued)

- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data in another sector within the same device
- **Extended Operating temperature range: –40°C to +85°C**

Please refer to “MBM29F200TA/MBM29F200BA” in detailed specifications.

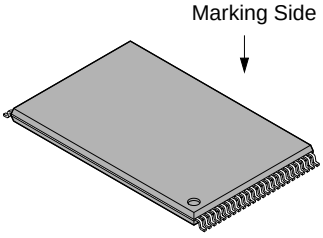
■ PACKAGE

44-pin Plastic SOP

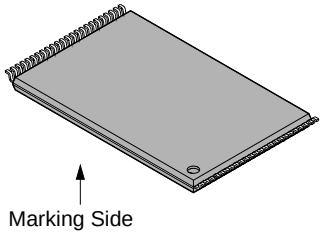


(FPT-44P-M16)

48-pin Plastic TSOP (I)



(FPT-48P-M19)



(FPT-48P-M20)

■ GENERAL DESCRIPTION

The MBM29F200TA-X/BA-X is a 2M-bit, 5.0 V-only Flash memory organized as 256K bytes of 8 bits each or 128K words of 16 bits each. The MBM29F200TA-X/BA-X is offered in a 44-pin SOP and 48-pin TSOP (I) packages. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The MBM29F200TA-X/BA-X offers access times 90 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29F200TA-X/BA-X is pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The MBM29F200TA-X/BA-X is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

A sector is typically erased and verified in 1.0 second (if already completely preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29F200TA-X/BA-X is erased when shipped from the factory.

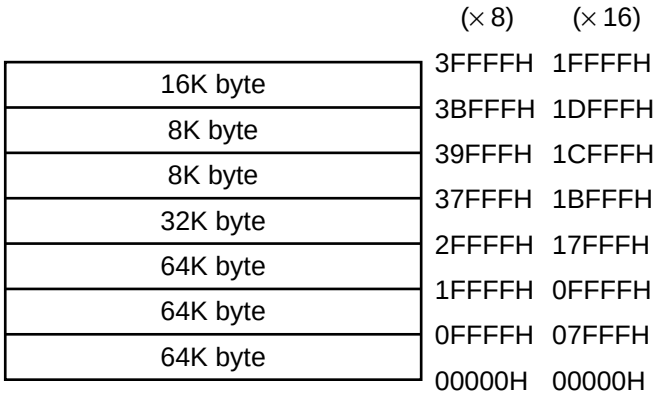
The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The MBM29F200TA-X/BA-X memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

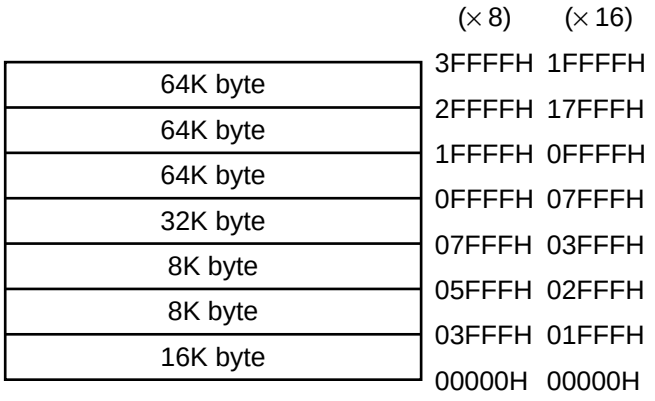
MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16K byte, two 8K bytes, one 32K byte, and three 64K bytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable.



MBM29F200TA-X Sector Architecture



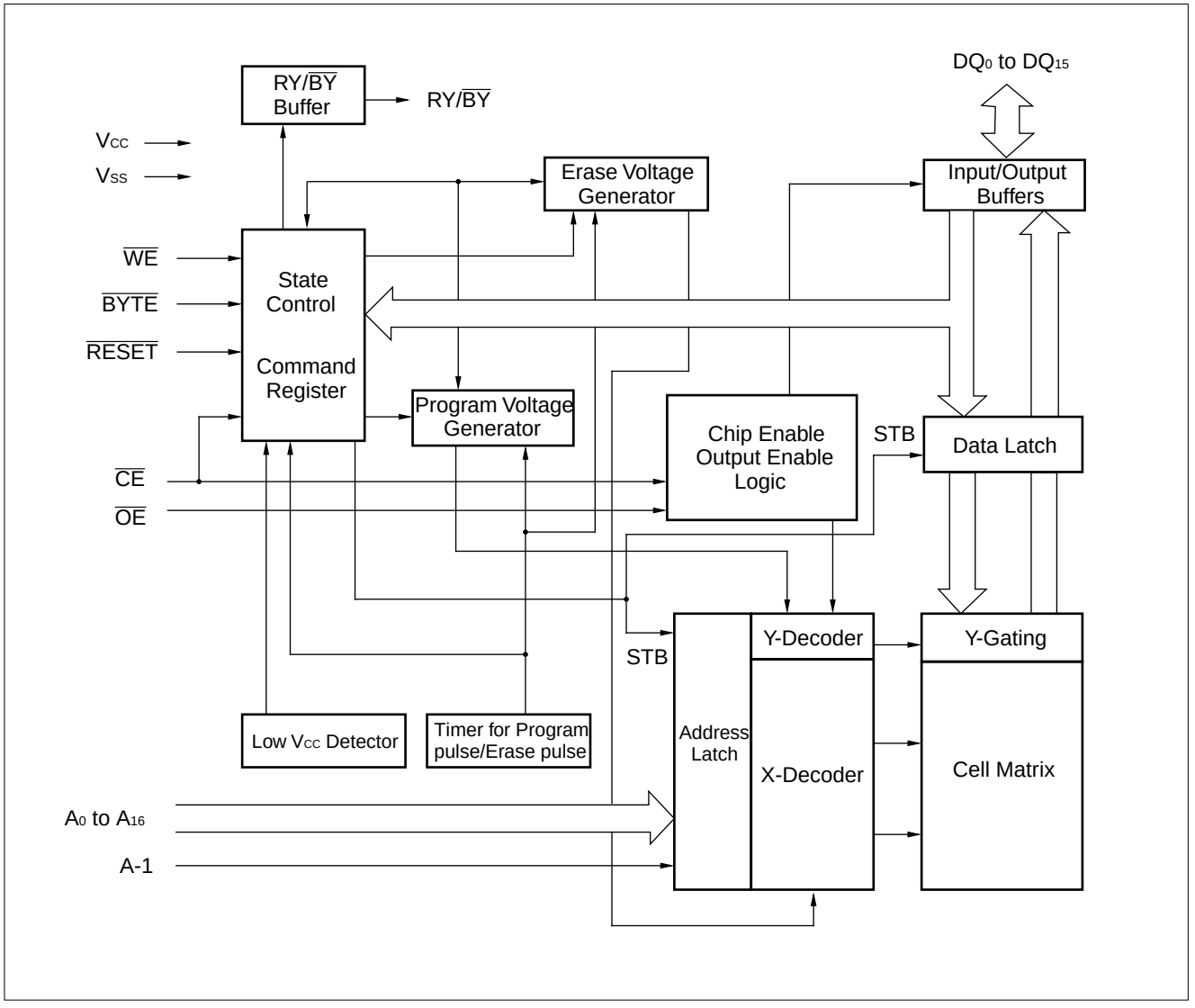
MBM29F200BA-X Sector Architecture

■ PRODUCT LINE UP

Part No.		MBM29F200TA-X/MBM29F200BA-X	
Ordering Part No.	V_{CC} = 5.0 V±10%	-90-X	-12-X
Max. Access Time (ns)		90	120
Max. $\overline{CE}$ Access Time (ns)		90	120
Max. $\overline{OE}$ Access Time (ns)		35	50

MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

■ BLOCK DIAGRAM

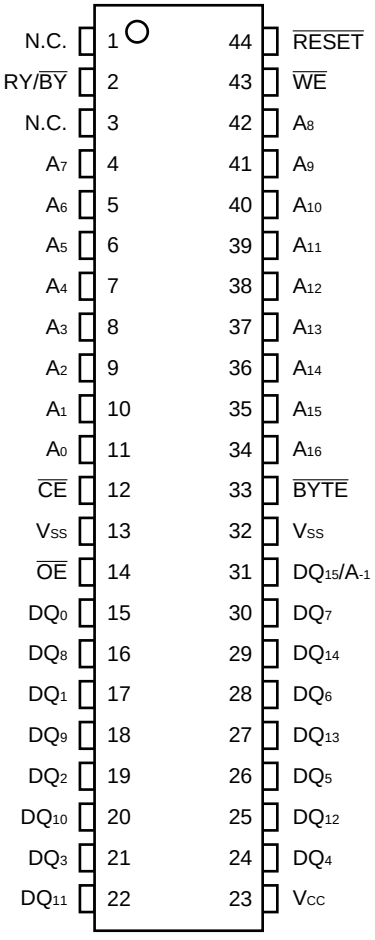


MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

■ CONNECTION DIAGRAMS

SOP

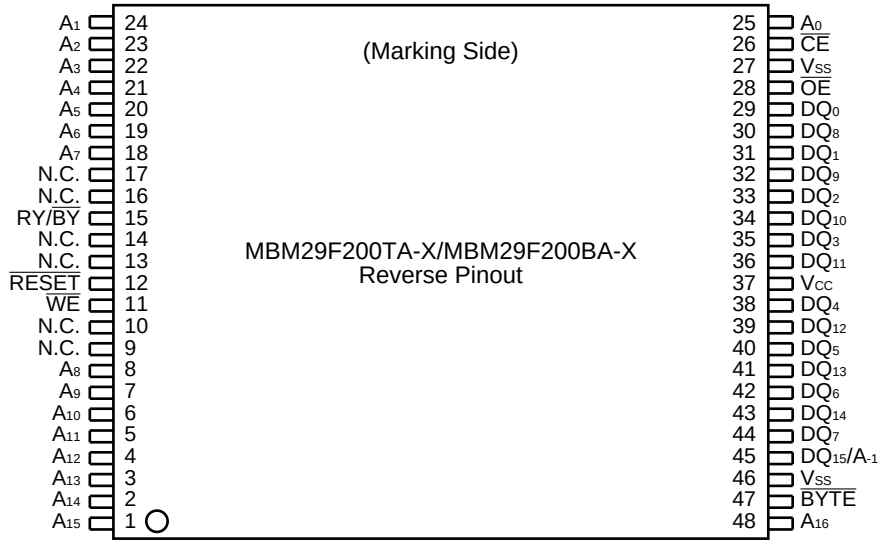
(Top View)



FPT-44P-M16

TSOP (I)

FPT-48P-M19



FPT-48P-M20

MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

■ LOGIC SYMBOL

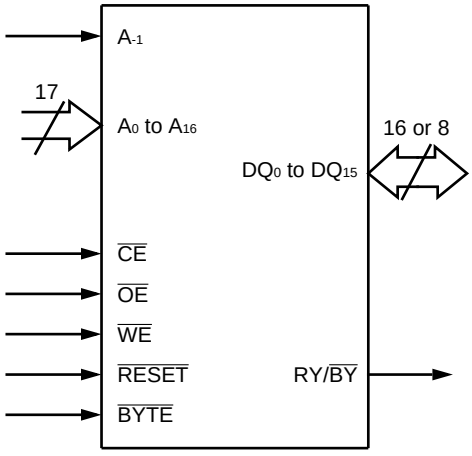


Table 1 MBM29F200TA-X/MBM29F200BA-X Pin Configuration

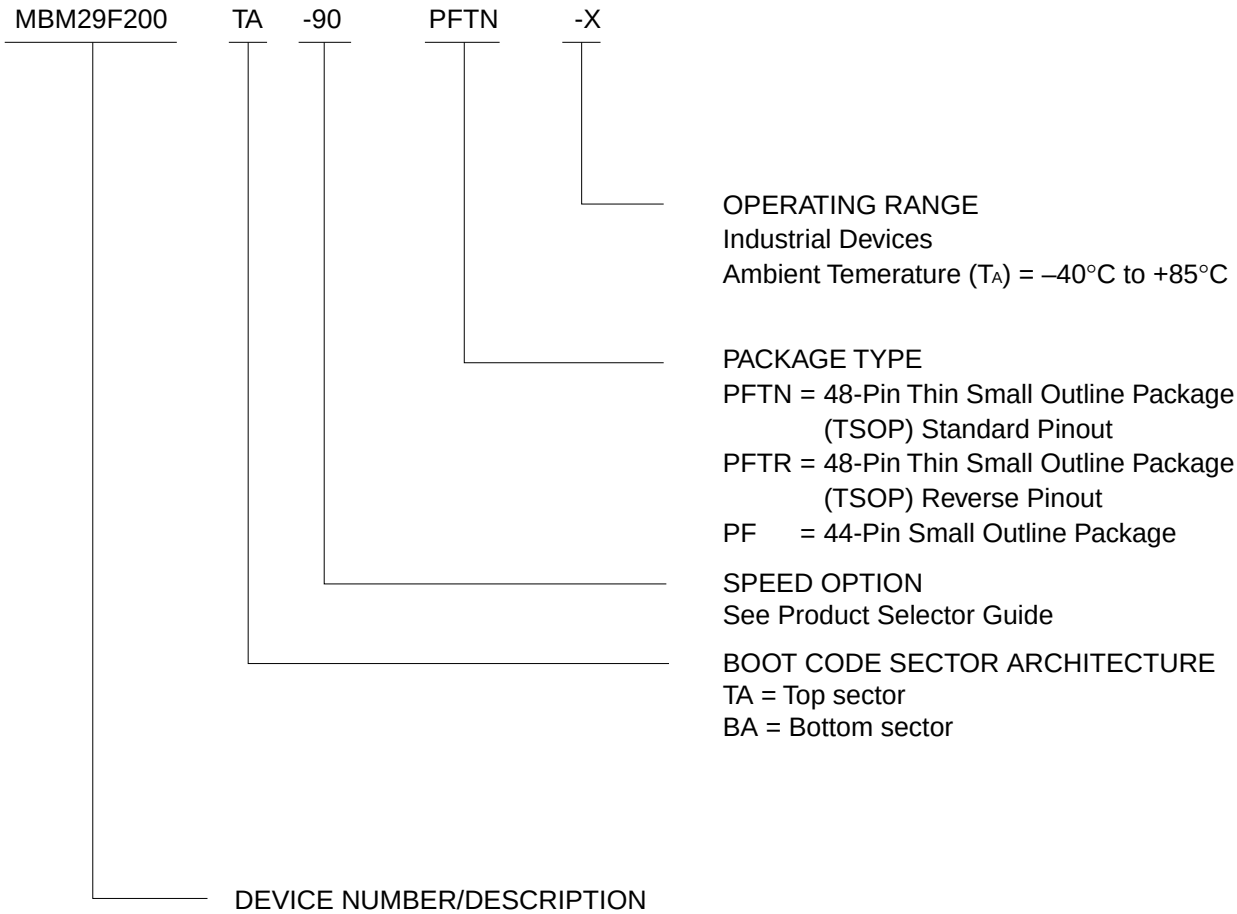
Pin	Function
A_{-1}, A_0 to A_{16}	Address Inputs
DQ_0 to DQ_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready-Busy Output
$\overline{RESET}$	Hardware Reset Pin/Sector Protection Unlock
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V±10%)

MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

■ ORDERING INFORMATION

Industrial Devices

Fujitsu industrial devices are available in several packages. The order number is formed by a combination of:



■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +125°C
Ambient Temperature with Power Applied..... –40°C to +85°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, $\overline{RESET}$ (Note 1)..... –2.0 V to +7.0 V
V_{CC} (Note 1) ..... –2.0 V to +7.0 V
A_9, $\overline{OE}$, $\overline{RESET}$ (Note 2) ..... –2.0 V to +13.5 V

Notes: 1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9, $\overline{OE}$, $\overline{RESET}$ pins are –0.5 V. During voltage transitions, A_9, $\overline{OE}$, $\overline{RESET}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, $\overline{OE}$, $\overline{RESET}$ pins are +13.0 V which may positive overshoot to 13.5 V for periods of up to 20 ns.

WARNING: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING RANGES

Industrial Devices
Ambient Temperature (T_A) ..... –40°C to +85°C

V_{CC} Supply Voltages ..... +4.50 V to +5.50 V

Recommended operating ranges define those limits between which the functionality of the device is guaranteed.

■ MAXIMUM OVERSHOOT

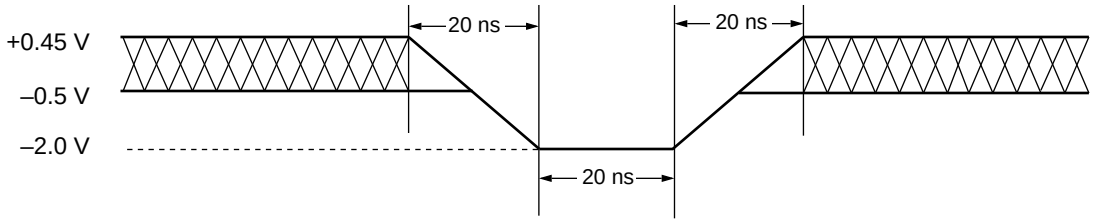


Figure 1 Maximum Negative Overshoot Waveform

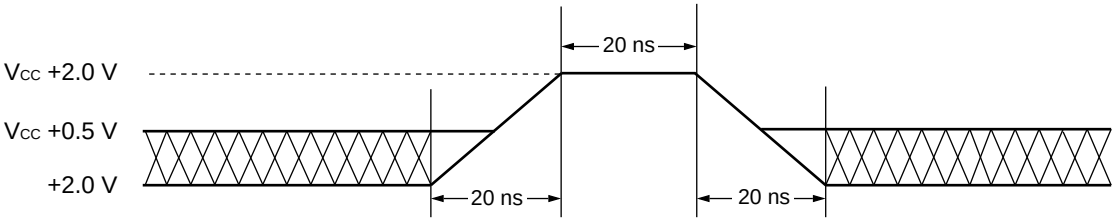
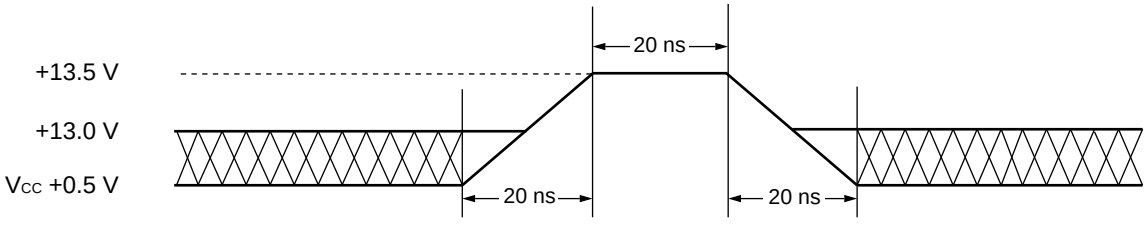


Figure 2 Maximum Positive Overshoot Waveform 1



Note : This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Positive Overshoot Waveform 2

■ DC CHARACTERISTICS

- **TTL/NMOS Compatible**

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		—	±1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		—	±1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max., A_9, $\overline{OE}$, $\overline{RESET}$ = 12.0 V		—	50	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte	—	50	mA
			Word		60	
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	80	mA
I_{CC3}	V_{CC} Current (Standby)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IH}, $\overline{RESET}$ = V_{IH}		—	1.5	mA
I_{CC4}	V_{CC} Current (Standby, Reset)	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{IL}		—	1.5	mA
V_{IL}	Input Low Level	—		–0.5	0.6	V
V_{IH}	Input High Level	—		2.4	V_{CC} +0.5	V
V_{ID}	Voltage for Autoselect, Sector Protection, and Temporary Sector Unprotection (A_9, $\overline{OE}$, $\overline{RESET}$)	V_{CC} = 5.0 V		11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 5.8 mA, V_{CC} = V_{CC} Min.		—	0.45	V
V_{OH}	Output High Voltage Level	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.		2.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—		3.2	4.2	V

Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz).
The frequency component typically is 2 mA/MHz.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

- **CMOS Compatible**

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		—	±1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		—	±1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max. A_9, $\overline{OE}$, $\overline{RESET}$ = 12.0 V		—	50	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte	—	50	mA
			Word		60	
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	80	mA
I_{CC3}	V_{CC} Current (Standby)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ±0.3 V, $\overline{RESET}$ = V_{CC} ±0.3 V		—	100	µA
I_{CC4}	V_{CC} Current (Standby, Reset)	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{SS} ±0.3 V		—	100	µA
V_{IL}	Input Low Level	—		–0.5	0.6	V
V_{IH}	Input High Level	—		0.7 × V_{CC}	V_{CC} +0.3	V
V_{ID}	Voltage for Autoselect, Sector Protection, and Temporary Sector Unprotection (A_9, $\overline{OE}$, $\overline{RESET}$)	V_{CC} = 5.0 V		11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 5.8 mA, V_{CC} = V_{CC} Min.		—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.		0.85 × V_{CC}	—	V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.		V_{CC} –0.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—		3.2	4.2	V

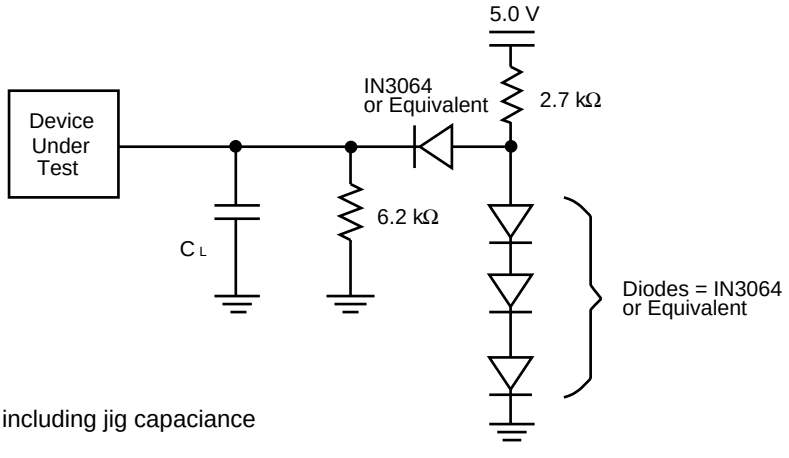
Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz).
The frequency component typically is 2 mA/MHz.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

■ AC CHARACTERISTICS

- **Read Only Operations Characteristics**

Parameter Symbols		Description	Test Setup		-90-X (Note 1)	-12-X (Note 1)	Unit
JEDEC	Standard						
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	Max.	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	Max.	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	0	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	Max.	20	20	µs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	Max.	5	5	ns

Note: Test Conditions- Output Load: 1 TTL gate and 100 pF
Input rise and fall times: 20 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 0.45 V and 2.4 V
Output: 0.8 V and 2.0 V



Note: C_L = 100 pF including jig capaciance

Figure 4 Test Conditions

- **Write/Erase/Program Operations**

Alternate $\overline{WE}$ Controlled Writes

Parameter Symbols		Description			-90-X	-12-X	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	ns
			Toggle and $\overline{Data}$ Polling	Min.	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min.	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min.	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	8	8	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1.5	1.5	sec
				Max.	30	30	sec
—	t_{VCS}	V_{CC} Setup Time		Min.	50	50	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)		Min.	4	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)		Min.	100	100	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
—	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	500	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z		Max.	30	30	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min.	35	50	ns

Notes: 1. This does not include the preprogramming time.
2. These timings are for Sector Protection operations.

- **Write/Erase/Program Operations**

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			-90-X	-12-X	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min.	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min.	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min.	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min.	0	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	ns
			Toggle and $\overline{Data}$ Polling	Min.	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min.	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min.	45	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min.	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	8	8	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note)		Typ.	1.5	1.5	sec
				Max.	30	30	sec
—	t_{VCS}	V_{CC} Setup Time		Typ.	50	50	µs
—	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	500	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z		Max.	30	30	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min.	35	50	ns

Note: This does not include the preprogramming time.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1.5	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time	—	8	500	µs	Excludes system-level overhead
Chip Programming Time	—	2.1	13	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

■ TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8.5	11.5	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	7.5	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8.5	11	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

MBM29F200TA-90-X/-12-X/MBM29F200BA-90-X/-12-X

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